REMARKS/ARGUMENTS

Applicants have received the Office action dated October 12, 2004, in which the Examiner: 1) rejected claims 2, 3, 9-16 and 27 under 35 U.S.C. § 112, second paragraph, as being indefinite; 2) rejected claim 1, 9 and 17 under 35 U.S.C. § 102(b) as being clearly anticipated by Sharangpani (U.S. Pat. No. 5,357,455); 3) rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Rault (U.S. Pat. No. [not given in Office action]) in view of Sharangpani; and 4) objected to claims 2, 4-8, 10-16 and 18-23 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

With this Response, Applicants amend claims 1-2, 4, 6-7, 9-11, 15-18, 20 and 27. Reconsideration is respectfully requested.

I. DRAWING AMENDMENTS

With this Response, Applicants amend the formal drawing Figures submitted May 22, 2002, as discussed above. No new matter is added.

II. AMENDMENTS TO THE SPECIFICATION AND TITLE

In response to the objection to the Title, Applicants suggest the following new title, "Method and System of a Microprocessor Subtraction-Division Floating Point Divider." Further, Applicants amend paragraphs [0006] and [0041] to correct typographical errors. Finally, Applicants correct the spelling of 'complement' in paragraphs [0028], [0032], [0036] and [0045]. No new matter is added.

III. OBJECTIONS TO THE CLAIMS

With this Response, Applicants amend claims 2, 3 and 27 as suggested by the Examiner. The requested amendment to claim 10 is moot given that claim 10 has been re-written into independent form. To address the concern regarding having only one most significant bit to the right of the radix point, Applicants amend claim 9 to call out a plurality. This amendment necessitates corresponding amendments to claims 10 and 11. Finally, Applicants correct the spelling of 'complement' in claim 11. No new matter is added.

IV. EFFECTIVELY ALLOWED AND ALLOWED CLAIMS

In the Office action dated October 12, 2004, the Examiner objected to claims 2, 4-8, 10-16 and 18-23. With this Response, Applicants amend claims 2, 4, 6-7, 10, 15-16, 18, and 20 to be in independent form (including the limitations of the base claim and any intervening claims). It is noted that each of these claims already contained these limitations by virtue of their previous dependency. Claims 5, 8, 11-14, 19 and 21-23 are dependent from the re-written claims. Thus, claims 2, 4-8, 10-16 and 18-23 should now be in a condition for allowance.

Applicants appreciate the allowance of claims 24-26 and 28-32. With the amendment to claim 27 above, this claim too should now be in a condition for allowance.

V. THE "RAULT" REFERENCE

The Office action dated October 12, 2004 rejects claim 3 as allegedly unpatentable over "Rault" and Sharangpani. However, the body of the Office action does not give a patent number or application serial number for Rault. Moreover, Rault was neither cited by Applicants in a form PTO-1449, nor is Rault listed in the attached form PTO-892. Applicants request that this fact be kept in mind when determining the finality of any subsequent action on the merits.

VI. CLAIM REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly anticipated by Sharangpani. Applicants amend claim 1 to remove much of the preamble wording. These amendments are not narrowing amendments.

Sharangpani is directed to a floating point remainder generator for a math processor. (Sharangpani Title). With regard to selecting quotient values for SRT division, and referring to Sharangpani's Figure 3, Sharangpani states:

> **Quotient predictor PLA 230 receives the most significant bits of the divisor** from partial remainder generator circuit 300 over signal lines 322. Carry propagate adder (CPA) 210 receives a truncated portion of the redundant partial remainder from partial remainder generator 300 over signal lines 365 and 369. CPA 210 assembles the sum portion 365 and carry portion 369 of the truncated partial

> remainder into composite partial remainder 212, which is input to multiplexer 220.

(Sharangpani Col. 4, lines 52-62 (emphasis added)). Thus, Sharangpani teaches using **the most significant bits from the partial remainder generator**, in part, to select the next quotient value.

Claim 1, by contrast, specifically recites, "calculating a carry-propagate form of a plurality of most significant bits to the right of the radix point of the unshifted partial remainder... ." Sharangpani does not teach or fairly suggest such a system. In particular, Sharangpani does not teach or fairly suggest "calculating a carry-propagate form of a plurality of **most significant bits to the right of the radix point** of the ... partial remainder." For this reason alone, claim 1 should be allowed.

Claim 1 further recites, "assigning a next quotient digit to be a whole number value of at least one of the most significant bits to the right of the radix point of the unshifted partial remainder." The quotient predictor PLA of Sharangpani bases its decision on a combination of the most significant bits of the divisor and a truncated portion of the partial remainder. (Sharangpani Col. 4, line 52 – Col. 5, line 30). Thus, Sharangpani does not assign "a next quotient digit **to be a whole number value of at least one of the most significant bits to the right of the radix point**... ." For this additional reason, claim 1 should be allowed.

Based on the foregoing, Applicants respectfully submit that claim 1, and claim 3 which depends from claim 1, should be allowed.

B. Claim 9

Claim 9 stands rejected as allegedly anticipated by Sharangpani. Applicants amend claim 9 to remove much of the preamble wording. The amendments to the preamble are not narrowing amendments. Claim 9 is also amended as noted above in Section III, and to more clearly define over Sharangpani's use of remainder portions in positions greater than the radix point.

Sharangpani is directed to a floating point remainder generator for a math processor. (Sharangpani Title). Sharangpani teaches using **the most**

significant bits from the partial remainder generator, in part, to select the next quotient value. (Sharangpani Col. 4, lines 52-62).

Claim 9, by contrast, specifically recites, "a decode logic coupled to the first carry-out, the second carry-out, and the plurality of most significant bits of the resultant in carry-propagate form, and wherein the decode logic selects the quotient digit to be the whole number value **of the plurality of most significant bits to the right of the radix point of the resultant** in carry-propagate form... ." Sharangpani does not teach or fairly suggest such a system. In particular, Sharangpani does not teach or fairly suggest that "the plurality of most significant bits to the right of the radix point of the resultant" should be used; rather, Sharangpani appears to teach using the most significant bits. Moreover, Sharangpani does not teach or fairly suggest "wherein the decode logic **selects the quotient digit to be the whole number value of the plurality of most significant bits to the right of the radix point of the resultant**... ." In Sharangpani, the selection appears to be based on combination of the most significant bits of the divisor and a truncated portion of the partial remainder. (Sharangpani Col. 4, line 52 – Col. 5, line 30).

Based on the foregoing, Applicants respectfully submit that claim 9 should be allowed.

C. Claim 17

Claim 17 stands rejected as allegedly anticipated by Sharangpani. Applicants amend claim 17 to remove much of the preamble wording. These amendments are not narrowing amendments.

Sharangpani is directed to a floating point remainder generator for a math processor. (Sharangpani Title). Sharangpani teaches using **the most significant bits from the partial remainder generator**, in part, to select the next quotient value. (Sharangpani Col. 4, lines 52-62).

Claim 17, by contrast, specifically recites, "calculating a carry-propagate form of a plurality most significant bits to the right of the radix point of the resultant, and the calculating the carry-propagate form also producing a second carry-out... ." Sharangpani does not teach or fairly suggest such a system. In

particular, Sharangpani does not teach or fairly suggest "calculating a carry-propagate form **of a plurality most significant bits to the right of the radix point** of the resultant... ." Rather, Sharangpani appears to teach using the most significant bits. For this reason alone, claim 17 should be allowed.

Claim 17 further recites, "assigning a next quotient digit to be a value directly indicated by at least one of the most significant bits to the right of the radix point of the resultant... ." The quotient predictor PLA of Sharangpani bases its decision on a combination of the most significant bits of the divisor **and** a truncated portion of the partial remainder. (Sharangpani Col. 4, line 52 – Col. 5, line 30). Thus, Sharangpani does not assign "a next quotient digit to be a value **directly indicated by at least one of the most significant bits to the right of the radix point of the resultant** ... ." For this additional reason, Claim 17 should be allowed.

Based on the foregoing, Applicants respectfully submit that claim 17 should be allowed.

VII. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including

fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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